Monolithic Switched-Capacitor DC-DC Towards High Voltage Conversion Ratios

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***Abstract*—Recent research has introduced switched-capacitor DC-DC converters with voltage conversion ratios (VCR) of up to 8. Their ability to implement any given voltage conversion ratio at a duty cycle of 50% shows promise to employ them in very high voltage conversion ratio applications. This is due to the fact that the VCR is a result of the switched-capacitor topology being used, instead of the Pulse Width Modulation (PWM) duty cycle as is the case with inductive DC-DC converters.**

This work aims to investigate the potential and feasibility of switched-capacitor topologies towards a monolithically integrated high voltage conversion ratio switched-capacitor DC-DC converter. Essential topology parameters and metrics that influence performance in this context are identified and their relation as function of the voltage conversion ratio is investigated. A comparison over a set of well-performing SC topologies yields a clear result, demonstrating a topology that circumvents technological weakness with topological strength and vice versa.

***Index Terms*—Fully integrated, switched-capacitor, high voltage conversion ratio, power converter, capacitive, DC-DC**

I. Introduction

The ever present voltage gap between a voltage source and a load requires DC-DC converters to efficiently bring source and load together. A typical voltage gap is present in handheld systems which are battery operated. Lithium Ion batteries exhibit terminal voltages of 2.8V-4.2V while the circuit supply voltage is roughly 1V. Alternatively, step-up conversion of the same voltage source can be required to generate the supply rail for a backlight LED driver. While the VCR of the former example remains low, the latter requires a higher VCR and deals with higher voltages as well. Other examples that typically require even higher VCR's include LIDAR, Power over Ethernet, ultrasound transmitter drivers, piezo actuators and drivers for MEMS applications.

Both an inductive as well as a capacitive approach is possible to implement the energy storage element, critical to a DC-DC converter's operation. Inductive DC-DC converters have the advantage over switched-capacitor DC-DC converters that they can implement a continuous VCR by means of PWM. But this also implies that the VCR is related to the PWM duty cycle and as such can become an issue towards high VCR. Even more so when taking into account that the switches in an inductive converter must be rated for the full input voltage, requiring high voltage devices which are more difficult to quickly turn on and off. This is in contrast to switched-capacitor DC-DC converters where the VCR is more determined by its topology, consisting of two specific capacitor configurations that are time alternated in a two-phase operation scheme in order to perform voltage conversion. Thus duty cycle can be kept at 50% regardless of the actual VCR. On top of that, single devices only need to block a fraction of the system rated voltage leading to a better device utilization [1].

Another strength of SC converters is their suitability for monolithic integration as they only require components native to an integrated circuit (IC) technology: switches and capacitors. Hereby eliminating component count limitations which would otherwise obstruct implementation practicality and feasibility of non fully-integrated solutions.

Despite the previous motivations to select the switched-capacitor DC-DC approach for high conversion ratios and this upwards/downwards to/from high voltage levels, current state of the art VCR's are limited to 8 [2] and many practical aspects that influence performance at high VCR are left unanswered. This work aims to investigate the combination of the aforementioned SC strengths into a monolithically integrated high voltage conversion ratio switched-capacitor DC-DC converter. To that end, performance and cost trade-offs are analysed for VCRs of a factor 10 and more, different implementation options are compared and the best candidate to use in high ratio and/or high voltage applications is selected. Only monolithic solutions are considered in order to maximize cost effectiveness of the proposed solution, which has its consequences on the solution space due to technology limitations on one hand but also possibilities on the other, related to the CMOS approach.

Section II will discuss the IC technology impact on DC-DC converters and the subsequent parameters necessary for comparison. Section III investigates popular topologies on the previously selected properties. Simulation results of the best candidate will be presented in Section IV, demonstrating performance and area cost trade-offs with respect to the voltage conversion ratio. Final conclusions are summarized in Section V.

II. Impact of CMOS Integration and Topology Comparison Parameters

Fully integrating a switched-capacitor DC-DC converter can be an attractive step as external board space and components are omitted. However, also limitations arise from choosing the monolithic approach. A switched-capacitor DC-DC converter relies on capacitors to store energy in its electric field and

switches to configure the capacitors in the physical topology configurations that result in a specific VCR, so the availablity and specifications of these basic components are shortly summarized in respect to power conversion applications. Fortunately the nature of CMOS integration allows, within a set of proces fabrication limits, a very flexibile layout. This freedom is an advantage of the monolithic approach, enabling custom designed structures and overcoming component count limitations.

A. Capacitors

Capacitors can be integrated in CMOS in quite a few ways, resulting in different specification parameters of which the capacitor voltage rating $V_{C,rated}$ $[V]$, capacitance density $C_{\square}$ $[\frac{fF}{\mu m^2}]$, parasitic coupling ratio to the substrate α_{par} $[\%]$ and the equivalent series resistance R_{esr} $[\Omega]$ are most crucial for application in DC-DC converters. The capacitor voltage rating increases with the spacing of the capacitor plates, and therefore is inversely related to capacitance density for both planar and non planar structures. Since α_{par} is the ratio of the parasitic substrate coupling capacitance to the net usable capacitance, it is inversely related to both the physical spacing of the capacitor structure to the substrate and and to its capacitance density. Lastly, R_{esr} is set by the resistance of capacitor plates, which are heavily layout dependent and thus a design parameter at the cost of capacitance density.

A more in depth overview of different types of fully integrated capacitors is summarized:

1) Gate Oxide: Gate oxide capacitors employ the planar thin or thick oxide normally used for making transistors. Densities typically range from 3-10$fF/\mu m^2$ depending on actual oxide thickness, consequently these capacitor voltage ratings coincide with the nominal voltage ratings for the thin and thick oxide transistors. The bottom plate is embedded in de substrate and thus subject to high substrate coupling, unless a Silicon On Insulator (SOI) proces is used. Despite the relatively high substrate coupling, α_{par} can still be small if the capacitance density is high. As gate oxides get thinner, they also become more susceptible to leakage current.

2) Metal-Insulator-Metal: MIM capacitors are widely available non standard planar structures, using a thin isolating layer with a higher dielectric constant than oxide to achieve very linear capacitors with capacitance densities typically in the range of 2-5$fF/\mu m^2$. Their voltage rating is about 2-3 times that of the gate oxide capacitors and is also fixed by the technology process. Due to their location higher up in the metal stack, they exhibit a very low parasitic ratio α_{par}.

3) Metal-Oxide-Metal: MOM capacitors are built with the regular metal stack, typically in a vertical parallel plate arragement with via's. The freedom in the spacing of the vertical plates allows for a custom designed capacitor voltage rating, which is the most differentiating feature of this type of capacitor. Alternatively selecting the lowest level to be part of the structure allows the parasitic coupling ratio to be varied. Generally a low α_{par} can be achieved by not using all metals down to the lowest, but consequently at low capacitance densities of 0.5-1$fF/\mu m^2$ depending on actual number of used metals and the plate spacing.

4) Deep Trenches: A non standard limited availability capacitor structure [3] that is able to attain ultra high capacitance densities of over 200$fF/\mu m^2$ due to its vertical orientation deeply rooted in the substrate, and as such virtually eliminates α_{par} simultaneously. Originating from embedded DRAM, these capacitors are typically engineered with low capacitor voltage ratings.

5) Ferroelectrics: These capacitors are planar non standard structures [4] like the MIM capacitors, but with limited availability. The principle is similar, but a ferroelectric insulator material allows for a higher capacitance density with respect to the MIM capacitor.

Only three of the above types remain if only widely available integrated capacitor structures are considered: gate oxide (GO), metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors. In this case it can be seen that low loss, low density capacitors with flexible high voltage rating are available in the form of MOM capacitors. Alternatively, GO and MIM capacitors allow low to medium loss, higher density capacitors but with a technology fixed lower voltage rating.

B. Switches

Considering power conversion applications where switches are either fully OFF or ON, the $Q_{gate}R_{on}$ is a useful technology specific figure of merit that demonstrates the required charge to reach a certain conductance in the ON state. Besides the standard thin oxide devices that are rated at the nominal technology supply voltage with the technology's minimal feature size gate length, a secondary type of device with a thicker oxide and larger minimal gate length to sustain higher voltages form the set of devices most effective to implement a power converter. The $Q_{gate}R_{on}$ is lower for the thin oxide devices, but may need to be stacked in series to construct a new switch structure that can withstand higher voltages at the cost of a more complex gate driver scheme. The same approach can be applied to the thick oxide devices, or a combination of thin and thick oxide devices allowing many possibilities for generating the right switch structure for the required blocking voltage. The more switches need to be stacked, the more complex the drive scheme must be to ensure no single switch is subject to an overvoltage and auxiliary supply rails are needed to perform correct gate driving.

Drain extended planar MOS devices can block higher drain-source voltages and form an alternative if switch stacking is no longer an option, but require extra processing steps.

C. Topology Comparison Parameters

Previous work [1] described a calculation model for SC converters in which the topology specific properties can be extracted in parameters to describe capacitor utilization (k_c) and switch utilization (k_s), which both influence the output impedance R_{out}. A low k_c leads to less required flying capacitance for a given R_{out} specification and consequently

yields smaller parasitic coupling losses. Therefore, topologies with a low k_c vector, represented by a low K_c value, are preferential over others regarding parasitic coupling C_{par} and power density.

Other work [5] introduced a metric M_{sw}, given in Eq. 1, that quantizes the combined loss impact of each of the flying capacitor's parasitic substrate coupling.

$$M_{sw} = \sum_i k_{c,i} V_{sw,par,i}^2 \tag{1}$$

The loss is quantized as function of the parasitic coupling voltage swing $V_{sw,par,i}$, inherent to two phase topology reconfiguration, and is weighed by the utilization $k_{c,i}$ of that flying capacitor. Combining these metrics enables to compare topologies and to evaluate their performance prospects towards higher VCR. Especially due to the integrated context, M_{sw} associated losses heavily impact performance as the parasitic coupling capacitance determined by α_{par} may be subject to very high swing and consequently is very lossy, as given by:

$$E_{sw,i} = \alpha_{par,i} C_{fly,i} V_{sw,par,i}^2 \tag{2}$$

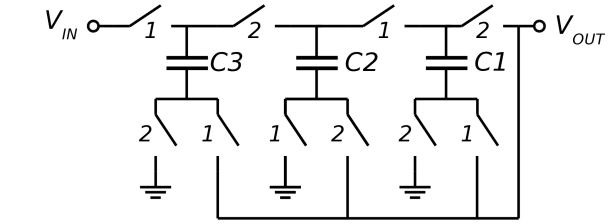
III. Topology Comparison

Many options are possible to implement a certain VCR, e.g. a single topology or a cascade. Cascading topologies, however, is to be avoided due to increased losses as result of having the cascade of converter output impedances in series. Cascading a topology can often be avoided by embedding it directly into the original converter topology, but may require an extra capacitor to preserve correct functionality, as is the case in Fig. 1(d).

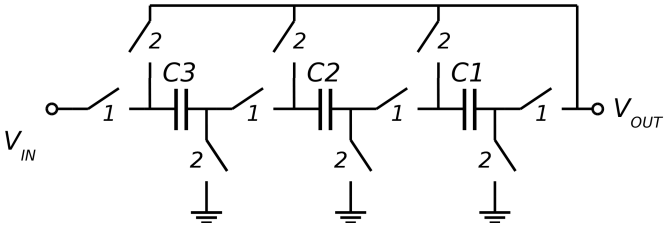
Switch utilization is less important than capacitor utilization efficiency in an integrated context because the typical low capacitance density of an integrated capacitor leads to a much bigger impact on the total die area compared to that of switches. Therefore Fig. 1 depicts topologies that are well known for their efficient capacitor usage and thus are integration friendly. Both Fig. 1(d) as well as 1(a) show a 4:1 Dickson Star topology, but 1(d) demonstrates the possibility to embed an additional 2:1 ratio at what would normally be the output of the regular 4:1 Dickson Star topology, without having the additional loss associated to converter cascading.

Table I lists the topology extracted parameters for comparison as function of voltage conversion ratio N. Vector k_c and its condensed result K_c show the capacitor utilization efficiency. A low K_c indicates that a topology is capacitor efficient and more importantly it can be seen that as the VCR becomes infinity, K_c converges to a low finite value. Even though capacitor utilization efficiency in this case does not take any area cost as result of the capacitor voltage rating into account, a valid comparison of the required capacitance is obtained. For all compared topologies, except the Doubler, this is even the lowest value theoretically possible and thus ideally suited for monolithic integration.

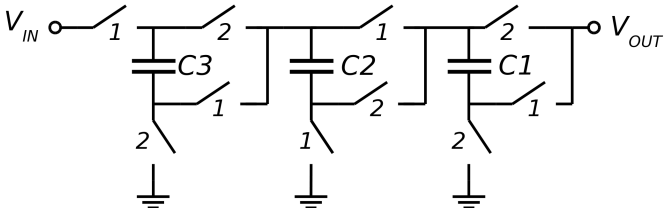
A more striking differentiation is shown by Table I in the parasitic swing metric M_{sw}. Topologies that structurally exhibit higher $V_{sw,par}$ values as the VCR increases, suffer a lot



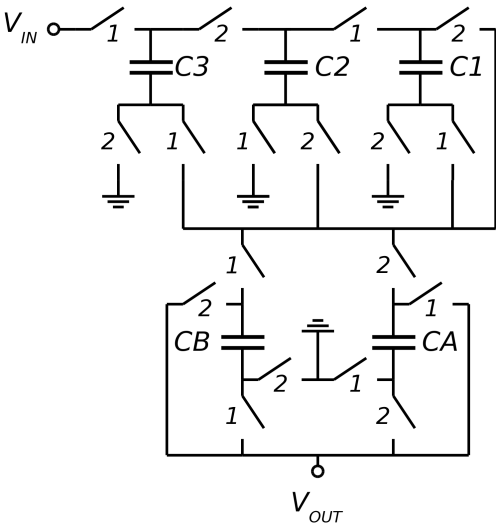
(a) Dickson star with ratio 4:1



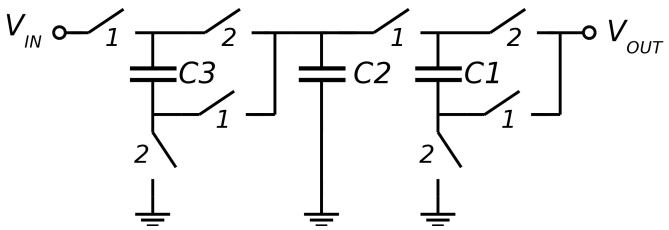
(b) Series parallel with ratio 4:1



(c) Fibonacci with ratio 5:1



(d) Dickson star embedded cascade with ratio 8:2:1



(e) Doubler with ratio 4:1

Fig. 1. Schematic representation of the topologies under comparison

TABLE I

LISTING OF TOPOLOGY SPECIFIC PARAMETERS AS FUNCTION OF VOLTAGE CONVERSION RATIO N REGARDING CAPACITANCE UTILIZATION K_c AND PARASITIC COUPLING METRIC M_{sw}, FOR THE TOPOLOGIES UNDER INVESTIGATION IN STEP-DOWN

	Dickson Star	Series Parallel	Fibonacci	Dickson Star Embedded Cascade	Doubler
Fig. #	1(a)	1(b)	1(c)	1(d)	1(e)
# columns = k	$k = N-1$	$k = N-1$	$Fib_{k+2} = N$ [a]	$k = \frac{N}{2} - 1$ [b]	$k = 2log_2(N) - 1$
k_c	$[\frac{1}{N} \cdots \frac{1}{N}]$	$[\frac{1}{N} \cdots \frac{1}{N}]$	$[Fib_1 \dots Fib_k]$	$[\frac{1}{N} \cdots \frac{1}{N}\ \frac{1}{4}\ \frac{1}{4}]$ [b]	$[\frac{1}{2}\frac{1}{2^2}\frac{1}{2^2}\frac{1}{2^3}\frac{1}{2^3} \cdots \frac{1}{2^N}\frac{1}{2^N}]$
$V_{C,rated,i}$ [V_{out}]	[1 2 3 ... N-1]	[1 ... 1]	$[Fib_2 \dots Fib_{k+1}]$	[2 4 6 ... ($\frac{N}{2}-1$) 1 1] [b]	[1 2 2 4 4 ... $\frac{N}{2}\frac{N}{2}$]
$V_{sw,par,i}$ [V_{out}]	[1 ... 1]	[1 2 3 ... N-1]	$[Fib_1 \dots Fib_k]$	[2 ... 2 1 1] [b]	[1 2^1 0 2^2 0 ... $2^{log_2(N)}$ 0]
M_{sw}	$\frac{N-1}{N}$	$\frac{1}{N}\sum_{i=1}^{N-1} i^2$	$\frac{1}{N}\sum_{i=1}^{k}(Fib_i)^3$	$2.5 - \frac{4}{N}$	$\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{i-1}$
$K_c = (\sum_{i=1}^{N} \lvert k_{c,i}\rvert)^2$	$(\frac{N-1}{N})^2$				$(\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{-i})^2$
$K_c,\ N=\infty$	1				2.25
$M_{sw},\ N=2$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$
$M_{sw},\ N=4$	$\frac{3}{4}$	3.5	–	1.5	1.5
$M_{sw},\ N=8$	$\frac{7}{8}$	17.5	4.62	2	3.5
$M_{sw},\ N=16$	$\frac{15}{16}$	77.5	–	2.25	7.5
$M_{sw},\ N=64$	$\frac{63}{64}$	1333.5	$N = 55-89$ 220.6 – 578	2.375	31.5
$M_{sw},\ N=\infty$	1	∞	∞	2.5	∞

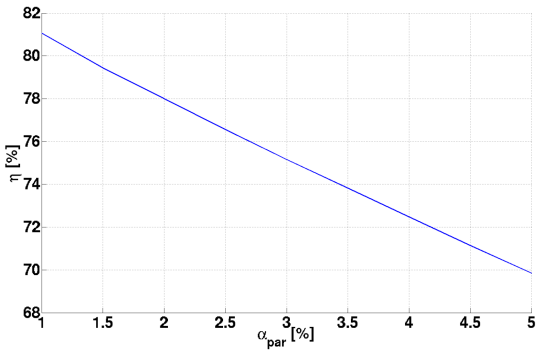
[a] $Fib_1 = 1, Fib_2 = 1$ [b] $N > 2$ and N even and $\frac{N}{2}$ even

since its associated losses are proportional to $V_{sw,par}^2$ as given by Eq. (2). Out of all compared topologies, the Dickson Star topology clearly outperforms all others as its M_{sw} metric not only converges, but does this to a very low finite value. On top of that, it must be noted that this M_{sw} value for infinite VCR is only twice that of the theoretical minimum at N=2. The Dickson Star topology hereby nearly eliminates the negative influence of rising VCR on overall converter performance and minimizes the influence of the parasitic substrate coupling inherent to the integrated circuit technology. Alternatively, IC technology is a good match for the incrementally varying $V_{c,rated}$ rating requirement of the Dickson Star topology as layout freedom in MOM capacitors allow them to custom fit the voltage requirement.

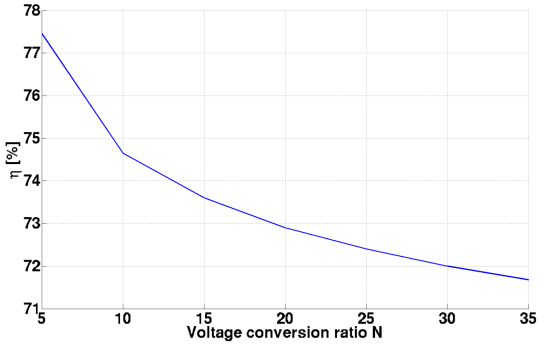
IV. SIMULATION RESULTS FOR DICKSON STAR TOPOLOGY

Section III demonstrated that the Dickson Star converter topology is the optimal choice for high voltage conversion ratios in a monolithically integrated context. Simulations of such a topology are shown in Fig. 2(a) and Fig. 2(b). The efficiency of an optimized Dickson Star converter with parasitic reduction and a VCR equal to 11 is shown in Fig. 2(a). The switching frequency is 10MHz and an ouput voltage/power of $3.3V/40mW$ is converted from a $41.7V$ input. The graph shows the efficiency as function of realistic parasitic coupling ratio α_{par} values. It can be seen that a range of 4% in α_{par} results in an efficiency decrease of 11%, emphasizing the impact of the parasitic substrate coupling in a monolithic SC converter.

Fig. 2(b) shows the simulated efficiency of a partially optimized converter with parasitic reduction as function of the voltage conversion ratio. As expected from Table I, the



(a) Dickson Star topology with parasitic reduction at VCR=11, $f_{sw} = 10$MHz, $V_{in} = 41.7V$, $V_{out} = 3.3V, P_{out} = 40$mW, $C_{tot} = 2.9nF$



(b) Evolution of the converter efficiency with rising voltage conversion ratio, $f_{sw} = 10$MHz, $\alpha_{par} = 3\%$, $V_{out} = 2.5V, P_{out} = 20$mW, $C_{tot}/V_{in} = 1.94nF/19V$ for N=5 to $2.86nF/100.5V$ for N=35

Fig. 2.

efficiency tends to converge as loss contributions stabilize due to the convergence of both K_c and M_{sw}, this while the VCR keeps increasing linearly. It is shown that efficiencies of above 70% are achievable at very high voltage conversion ratios if an α_{par} of 3% is reached. Designing capacitor structures to yield low parasitic coupling ratios will be a trade-off between low α_{par} and low die area, thus performance versus chip cost. Achieving low parasitic coupling is simplified in technologies such as Silicon On Insulator (SOI) allowing higher performance per area, but at an increased base cost for the technology.

A final set of simulation results is given in Fig. 3(a) - 3(d), showing the influence of the physical implementation consequences resulting from the flying capacitor voltage rating requirements. As the VCR increases, so do the capacitor voltage ratings of the flying capacitors related to the VCR increase. Once the average capacitor voltage rating increases beyond the fringe capacitor nominal rating, additional capacitor terminal spacing is required and both α_{par} and the average area density of C_{fly} are influenced, as can be seen in Fig. 3(a) and Fig. 3(b) respectively. Hereby, the efficiency of a typical Dickson Star converter with increasing VCR will not converge as in Fig. 2(b), but is shown in 3(c). Even though there is no actual convergence trend, good efficiency can be obtained at high VCR if α_{par} can be kept low. Fig. 3(d) demonstrates the corresponding power density $-$ VCR relation at $V_{out} = 1.8V$.

V. Conclusions

The Dickson Star topology is shown to be superior to the other topologies due to the convergence of both K_c and M_{sw} at very low values, hereby enabling monolithic SC DC-DC converters with very high voltage conversion ratios to be implemented with attractive efficiency and demonstrating that SC converters are indeed good candidates for high VCR applications provided the feasibility to keep $\alpha_{par,average}$ low.

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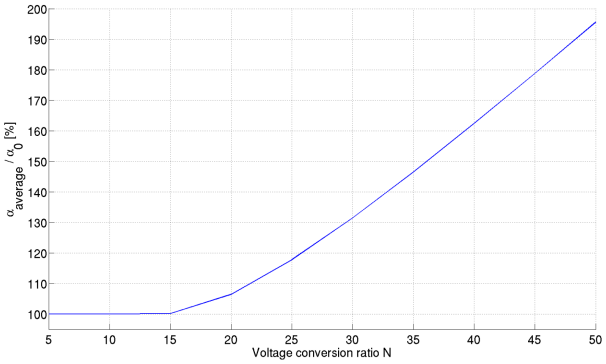
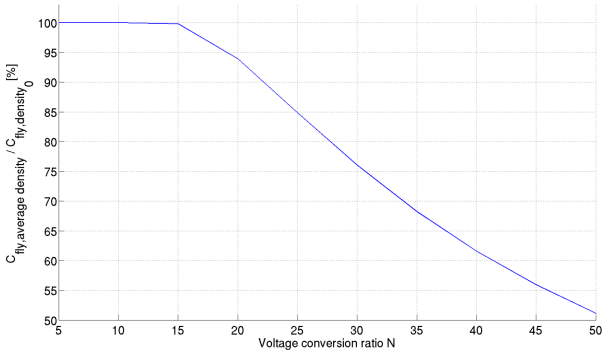
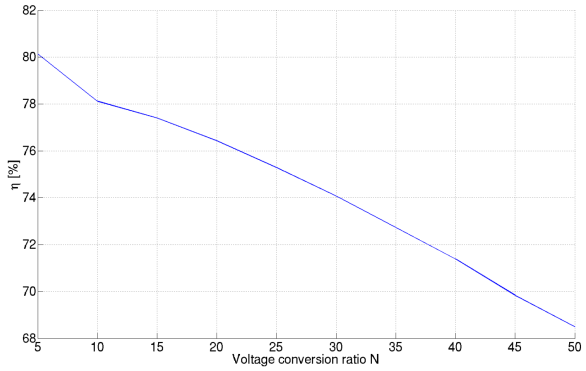


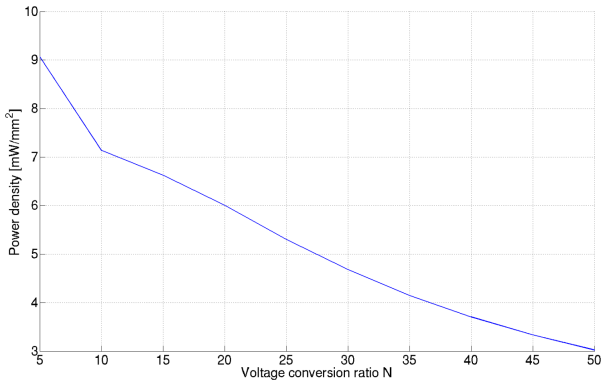
(a) $\alpha_{par,average}$,normalized to $\alpha_{par,0}$, as function of the VCR for a Dickson Star topology, $f_{sw} = 15$MHz, $V_{out} = 1.8V, P_{out} = 20$mW



(b) $C_{fly,average\ density}$,normalized to $C_{fly,density_0}$, as function of the VCR for a Dickson Star topology, $f_{sw} = 15$MHz, $V_{out} = 1.8V, P_{out} = 20$mW



(c) η as function of the VCR for a Dickson Star topology, $f_{sw} = 15$MHz, $V_{out} = 1.8V, P_{out} = 20$mW



(d) Power density as function of the VCR for a Dickson Star topology, $f_{sw} = 15$MHz, $V_{out} = 1.8V, P_{out} = 20$mW

Fig. 3.